Invited Paper

Progress in high-power high-efficiency VCSEL arrays

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ABSTRACT

We present recent results on high-power, high-efficiency two-dimensional vertical-cavity surface-emitting laser (VCSEL) arrays emitting around 808nm. Selectively oxidized, top-emitting single VCSEL emitters with 49% power conversion efficiency were developed as the basic building block of these arrays. Because of the strong GaAs absorption at the 808nm wavelength, the traditional bottom-emitting, substrate-emission configuration is not possible for large arrays that require efficient heat dissipation. The processing and packaging challenges are discussed. We demonstrate 3mm x 3mm arrays and 5mm x 5mm arrays with the GaAs substrate completely removed and mounted on diamond submounts. These arrays emit more than 50W and 120W, respectively, and exhibit a maximum power-conversion efficiency of 42%.

Keywords: Semiconductor lasers, vertical-cavity surface-emitting lasers (VCSELs), 808nm, high efficiency, high-power, 2D array, pumping, solid-state laser, frequency doubling, reliability.

1. INTRODUCTION

It was shown in [1] that vertical-cavity surface-emitting lasers (VCSELs) can be used as very high-power sources by fabricating large two-dimensional (2D) arrays of low-power, high-efficiency single-emitters. These high-power VCSEL sources present many advantages that include low-cost manufacturing [2], reliability [3], and good spectral and beam quality. Furthermore, unlike edge-emitters, VCSELs do not suffer from catastrophic optical damage (COD) [4], which means VCSELs can be operated reliably at high temperatures [5], eliminating the need for a refrigeration unit in some applications.

A wavelength of significant interest for high-power laser sources is 808nm. Such laser sources are used in industrial end-pumped DPSS lasers (Nd:YAG or Nd:YVO4) for end uses such as material cutting and processing, light welding, marking and printing [6]. Pump sources at 808nm are also used for green laser systems in which a multimode 808nm high-power source is used to pump Nd:YVO4 glass or a semiconductor gain medium set up in an external-cavity configuration to generate a single-transverse mode at 1064nm. Green light (532nm) is then obtained by intra-cavity second harmonic generation using a frequency doubling crystal (such as ppLN) located inside the cavity. These can be fabricated in very compact modules as part of RGB sources for micro-projectors for example [7]. Diode pumped green lasers are also used in many other applications such as scientific instruments (interferometers), precision machining, targeting in defense applications, and for fluorescence diagnostics and spectroscopic applications in the medical field.

There are very few reports in the literature discussing 808nm VCSELs [8]. One possible explanation for this lack of interest in 808nm VCSELs is that historically VCSELs have been mostly confined to low-power applications (a few mW at most), such as high-speed data transmission [9,10], whereas applications for 808nm semiconductor lasers require high powers.

In this paper we present several new results on 808nm VCSELs and high-power 808nm 2D VCSEL arrays. First, we present high-efficiency and high single-mode power results for top-emitting single devices. Second, we describe the processing and packaging steps involved in fabricating large 2D 808nm VCSEL arrays. Compared to the 976nm wavelength for example, the 808nm wavelength presents the additional challenge that substrate-emission is not an option because of the strong GaAs absorption at that wavelength. Therefore a bottom-emitting configuration such as is used for high-power 976nm VCSEL arrays for efficient heat dissipation [1] is no longer possible and the GaAs substrate needs to be removed. Finally, we present results on 3mm x 3mm and 5mm x 5mm arrays mounted on diamond submounts.

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2. HIGH-EFFICIENCY 808NM VCSEL SINGLE DEVICES

2.1 Device structure & fabrication

Epitaxial VCSEL material designed to lase around 808nm was grown on N-type GaAs substrate using MOCVD. Top-emitting single devices of different diameters were processed. A schematic of a single device is shown in Figure 1.

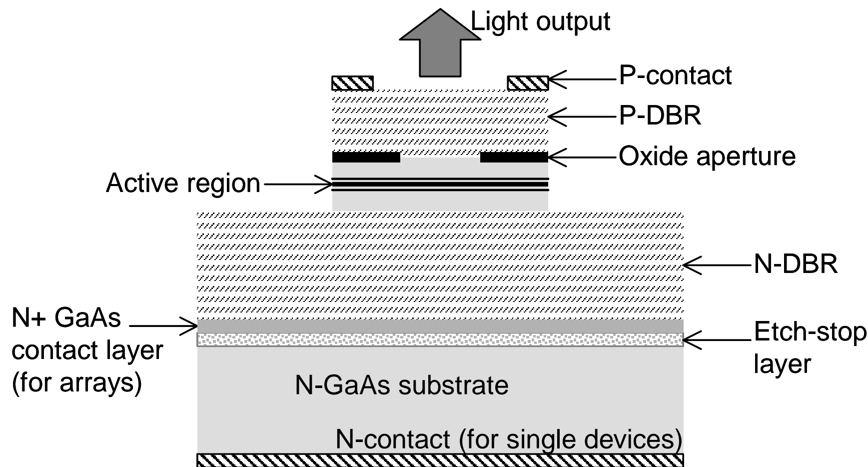


Fig. 1. Schematic of the selectively oxidized, top-emitting 808nm VCSEL structure.

For current and optical confinement, the selective oxidation process [11] is used to create an aperture near the active region to improve performance [12]. The growth starts with an etch-stop layer to facilitate substrate removal for processing of arrays as explained in the next section. Following the etch-stop layer is a highly doped N-GaAs layer that is used for the N-contact of the arrays. Then, an AlGaAs N-type high-reflectivity distributed Bragg reflector (DBR) follows. The active region consists of InAlGaAs strained quantum wells designed for 808nm emission, and is followed by P-type DBR output mirror, whose reflectivity is optimized for maximum PCE [13]. A high-Aluminum content layer is placed near the first pair of the P-DBR to later form the oxide aperture. The placement and design of the aperture is critical to minimize optical losses [14,15] and current spreading [16]. Band-gap engineering (including modulation doping) is used to design low-resistivity DBRs with low-absorption losses [17].

The processing of top-emitting single devices is straightforward. On the epitaxial side, Ti/Pt/Au ring contacts of different dimensions are evaporated to form the P-type contacts, which at the same time help act as the self-aligned mask for subsequent dry-etching (RIE) of mesas, deep enough to expose the Aluminum-rich layer. The samples are then exposed to high humidity in a furnace (390~420°C) for the selective oxidation process. On the substrate side, Ge/Au/Ni/Au metals are evaporated to form the N-contact. The devices are then probe tested at the wafer level.

2.2 Results and discussion

Individual devices are tested on a probe-station using a calibrated integrating-sphere/detector/power-meter system (Newport), a calibrated high-precision current source (ILX), and a calibrated voltmeter (Agilent). A TEC-controlled stage maintains a constant heat-sink temperature. A four-point-probe measurement was used to record the voltage accurately. For accurate determination of the device PCE, precise calibration of the instruments is critical. For example, for devices with small threshold currents (<1mA), a small offset in the current source could result in a significant error in PCE for these devices. We continually cross-check our results using different sets of instruments. Also, as a participant of the DARPA Super-High Efficieny Diode Source (SHEDS) program we were able to calibrate our instruments against NIST's own results on our devices. As a result, we were able to improve the measurement error of our test set-up to better than +/-1%.

Figure 2 shows the L-I-V characteristics of a 15µm-diameter device at room temperature. Threshold current, differential slope efficiency, and differential resistance are 0.98mA, 75.2%, and 65.7Ω, respectively. A maximum PCE

of 49.2% is achieved at 6.0mA (5.8mW). To the best of our knowledge, this is the highest PCE achieved to date for a top-emitting 808nm VCSEL device.

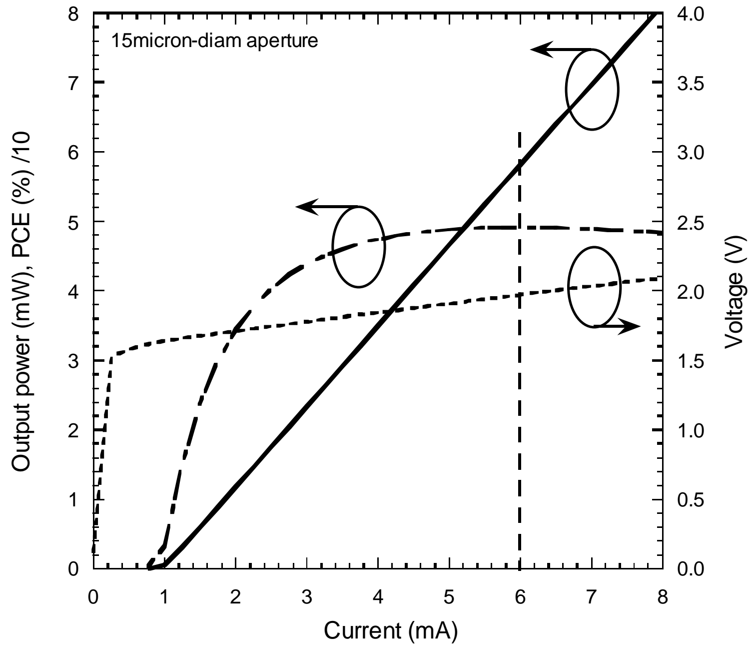


Fig. 2. L-I-V characteristics of a high-efficiency, top-emitting, 808nm VCSEL device. The oxide aperture diameter is 15µm. A maximum PCE of 49.2% is achieved.

We also grew different material and fabricated devices optimized for high single-mode power operation, while still maintaining a reasonable efficiency level. Results for a 4mircon-diameter device are shown in Figure 3.

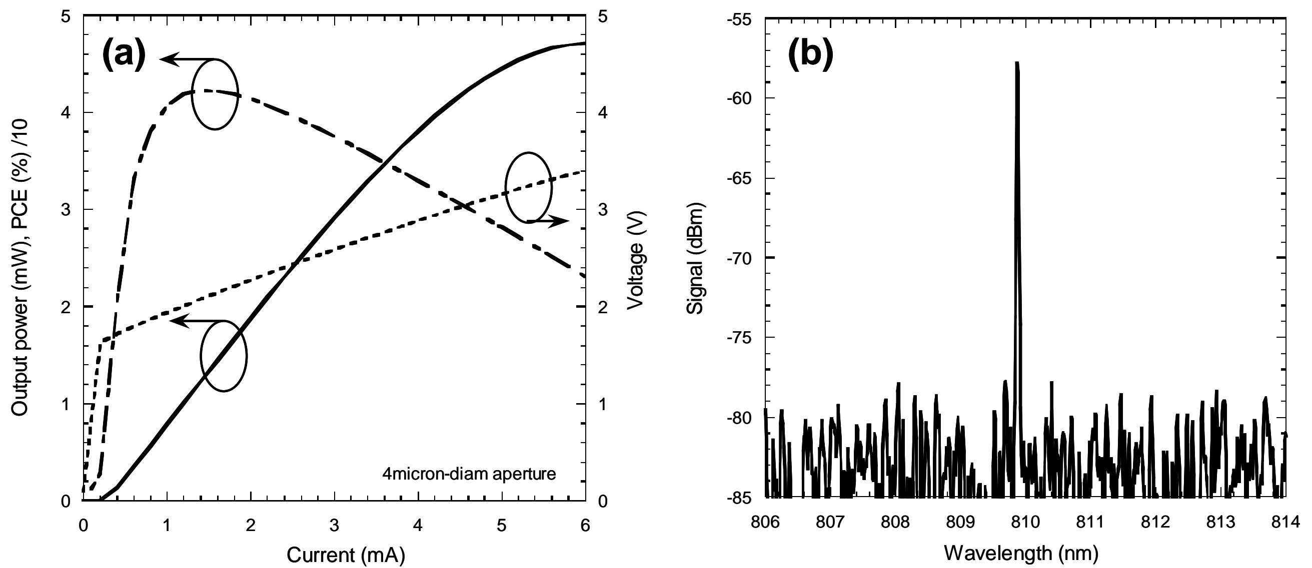


Fig. 3. (a) LIV characteristics of a 4micron-diameter 808nm VCSEL device, and (b) spectrum at roll-over.

The device remains single-mode across the entire operating range from threshold up to roll-over, to a maximum of 4.7mW single-mode power at roll-over. The peak power-conversion efficiency for this device is still high (42% at 1.2mW single-mode output power). Such devices are key to achieving high-brightness arrays, such as demonstrated in [1].

It is interesting to note that overall, the power conversion efficiency numbers are similar to the ones demonstrated for 976nm VCSELs in [1]: 51.2% and 49.2% for multimode 976nm and 808nm devices, respectively; and 44% and 42% for single-mode 976nm and 808nm devices, respectively. Because of the increased absorption below ~20% Aluminum in AlGaAs layers at 808nm, GaAs cannot be used as the high-index layer resulting in lower contrast DBRs, which increases the number of pairs required to achieve a certain reflectivity. For given doping levels, reducing the contrast between DBR layers also increases the field penetration depth in the DBRs, which increases absorption losses [18]. However, using lower contrast DBR layers usually means that the barrier resistance between the low and high index DBR layers will decrease, giving some room to lower the doping levels and therefore the absorption losses, especially in the P-DBR – this can compensate the negative effects of a low contrast DBR. Therefore, we believe that it is possible to maintain the high PCE levels for VCSELs across a broad wavelength range (~790-1100nm).

As in [1], to analyze the results of the high-PCE material (Fig. 2), we extend the work of Bour and Rosen [19] to VCSELs to obtain a simple analytical expression for the maximum PCE of a device as a function of the slope efficiency, threshold current, and resistance:

$$\eta_{e,m} = \eta_d \frac{V_v}{V_0}\left(1 - \frac{2}{1+\sqrt{1+\alpha}}\right) \tag{1}$$

where η_d is the differential slope efficiency, V_v is the photon energy voltage (1.534V for 808nm lasers), V_o is the zero-current intercept of the linear portion of the laser I-V characteristic (also referred to as the “turn-on voltage”), and α is a characteristic device parameter defined as $\alpha=V_0/(I_{th}R_d)=V_0/(J_{th}\rho_d)$, where I_{th} (J_{th}) and R_d (ρ_d) are the threshold current (threshold current density) and the resistance (resistivity) of the device considered, respectively.

Then, to model the size dependence of the threshold current, resistance, and slope efficiency, we also mimic the approach given in [1].

First, the size-dependent analytical expressions for the threshold current and slope efficiency derived by Hegblom et al. are used [16]. These take into account current and carrier spreading, which are a major contributor to loss of performance. These expressions are given by:

$$I_{th} = J_{\inf}\pi r_a^2 + \frac{I_0}{2} + r_a\sqrt{\pi I_0 J_{\inf}} \tag{2}$$

$$\eta_d = \eta_{\inf}/\left(1 + D_0/D_a\right) \tag{3}$$

where r_a (D_a) is the device aperture radius (diameter), I_0 is a characteristic spreading current, D_0 is a characteristic spreading distance, and J_{inf} and η_{inf} are the threshold current density and differential slope efficiency without spreading (infinitely large aperture), respectively. The parameters J_{inf} and η_{inf} depend only on the structure intrinsic parameters, such as the mirror reflectivities, the internal loss (that can include such effects as aperture scattering losses for very small devices), the number of quantum wells, the confinement factor, the internal quantum efficiency and material gain parameters. Analytical expressions for J_{inf} and η_{inf} can be found in [20] for example.

Then, the size-dependent resistance is modeled as the sum of two resistances in series, as is appropriate for a top-emitting structure with a P-DBR as the output mirror [1,21]:

$$R_d = R_L + R_V = \frac{\rho_{\inf}}{2\pi r_a} + \frac{\rho_0}{\pi r_a^2} \tag{4}$$

where ρ_{inf} (Ω.cm) and ρ_0 (Ω.cm^2) are characteristic resistivities. The first term R_L accounts for constriction or spreading, lateral and contact resistance (scales inversely with aperture perimeter) while the second R_V term models a uniform vertical current flow resistance (scales inversely with aperture area).

Figure 4 plots the threshold current, the resistance, and the differential slope efficiency as a function of device diameter D_a for high-efficiency top-emitting 808nm VCSEL devices. Equations (2), (3), and (4) are used to fit the data.

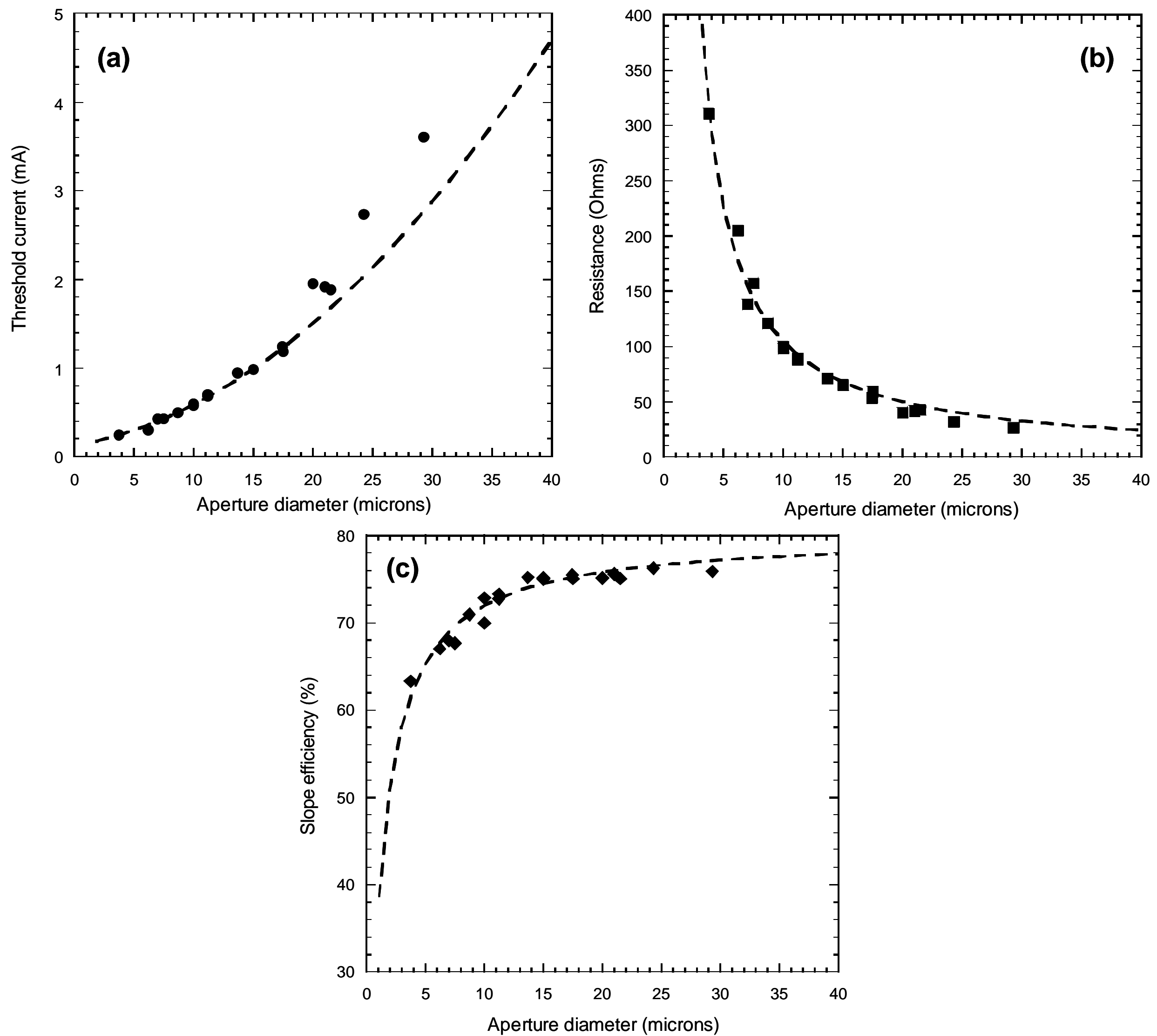


Fig. 4. (a) Threshold current, (b) resistance, and (c) differential slope efficiency as a function of device aperture diameter. The symbols are measured data and the lines represent best fits to using the analytical formulas.

Because these single devices were processed as top-emitters without any thinning of the substrate or adequate heat-sinking, some excessive heating induced effects can be seen for larger diameters (>20microns) compared to the expected trend: increase in threshold current, decrease in resistance, and decrease in slope efficiency. The fit for small diameters (<20microns) is very good.

The extracted characteristic parameters for this structure are given in Table 1. As in [1], these seven parameters are sufficient to fully characterize a particular structure in terms of PCE performance.

Table 1. Extracted VCSEL characteristic parameters from the fits in Figure 4.

Description	Symbol	Value	Unit
Turn-on voltage (zero-current intercept)	V_0	1.58	V
Threshold current density (infinite aperture size)	J_{inf}	290	A/cm^2
Characteristic spreading current	I_0	0.24	mA
Vertical resistivity	ρ_0	6.44e-6	$\Omega.cm^2$
Lateral resistivity	ρ_{inf}	0.303	Ω.cm
Characteristic spreading diameter	D_0	1.14	µm
Slope efficiency (infinite aperture size)	η_{inf}	80.1	%

Using these extracted parameters and the measured value V_0=1.58V (roughly independent of device size), α and $\eta_{e,m}$ (maximum PCE) are plotted against the measured data (Fig. 5).

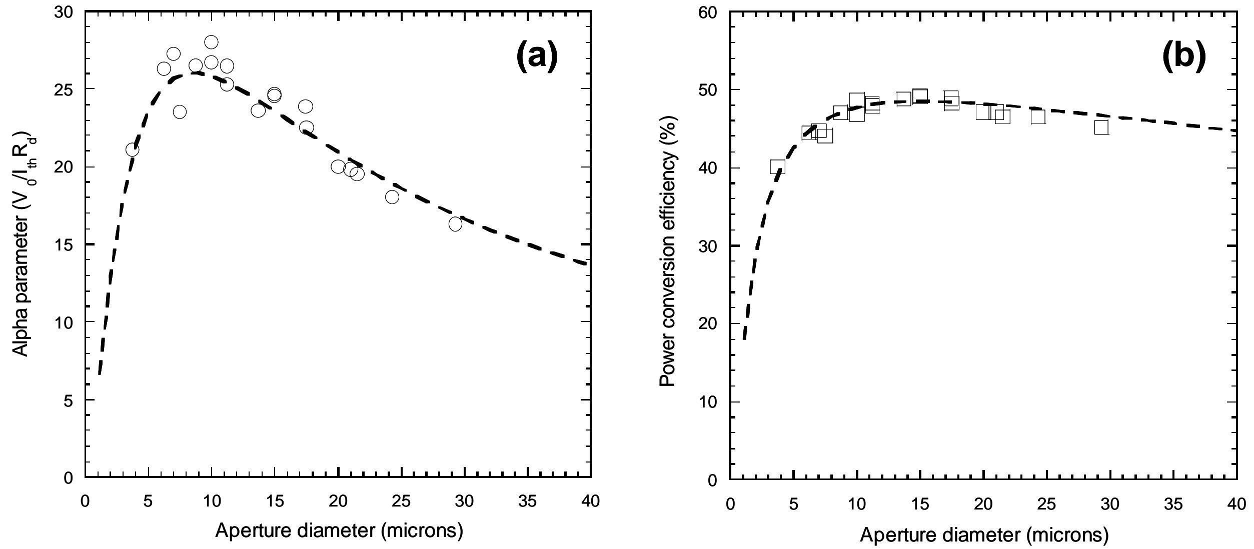


Fig. 5. (a) α-parameter and (b) maximum PCE as a function of device aperture diameter. The symbols are data and the lines were obtained using the analytical expressions and the parameters extracted in Table 1.

As can be seen in this case, α and $\eta_{e,m}$ have optimal values. The PCE characteristic is relatively flat (~49%) over the range 10~20micron-diameter. Higher PCE could potentially be obtained for diameters >20microns for properly processed devices (substrate removed and mounted on high thermal conductivity submounts).

For these top-emitting devices, the asymptotic expressions for α and $\eta_{e,m}$ (infinitely large diameters) are inversely proportional to the aperture diameter:

$$\alpha_{\text{inf}} = \frac{4V_0}{J_{\text{inf}}\,\rho_{\text{inf}}\,D_a} \tag{5}$$

$$\eta_{e,\text{inf}} = \eta_{\text{inf}}\,\frac{V_v}{J_{\text{inf}}\,\rho_{\text{inf}}\,D_a}\,. \tag{6}$$

and therefore converge towards zero for large diameters. This is in contrast to the behavior for the bottom-emitting 976nm devices reported in [1] for which α and $\eta_{e,m}$ converged towards constant values, not very different from their peak values. The difference comes from the scaling of the resistance with large diameters: in the case of the bottom-emitting structure (the P-DBR is the high reflector), the resistance is inversely proportional to the area for large diameters, whereas for the top-emitting structure (the P-DBR is the output mirror), the resistance is inversely proportional to the diameter for large diameters, which eventually limits the PCE. Hence, in the present top-emitting devices, the lateral resistivity ρ_{inf} becomes the limiting factor to achieving high PCE for large diameters.

Similarly to the devices described in [1], we found that the main obstacle to achieving high efficiency in these top-emitting VCSELs is lateral carrier diffusion in the active region, especially for these small aperture sizes.

3. 808NM VCSEL ARRAY FABRICATION

For high-power operation, efficient heat-removal is required. However, unlike 976nm high-power VCSEL arrays, a junction-down, bottom-emitting (substrate-emission) configuration is not possible for 808nm, because of the excessive GaAs substrate absorption at that wavelength. Furthermore, a top-emitting configuration with the GaAs substrate still present (even if thinned down) would add excessive thermal impedance. Therefore, in the case of 808nm VCSEL arrays, the GaAs substrate needs to be removed. This Section describes the processing and packaging steps of these high-power 808nm VCSEL arrays.

First, the epitaxial side of the sample is fully processed as shown in Figs. 6 and 7(a). Processing of 2D VCSEL arrays is similar to that of single devices. There are a few more processing steps such as plating of the N- and P-contacts for uniform current distribution within the array. A cross-section schematic of the processed epitaxial side of the sample is shown in Figure 6.

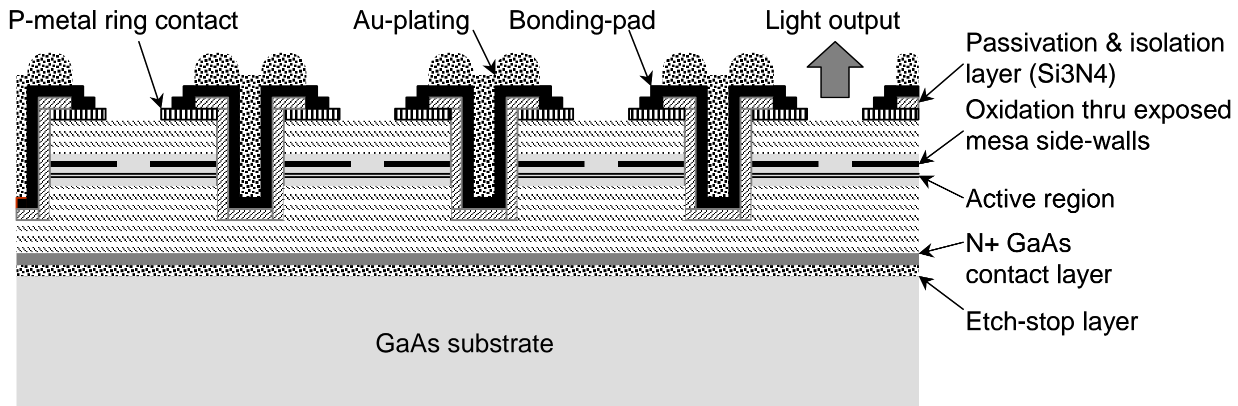


Fig. 6. Schematic cross-section of a 2D VCSEL array with the epitaxial side fully processed.

At this stage, the arrays are tested at the wafer level (before cleaving and separation) to check for performance and excessive "dead pixels" for example.

Then, the process continues with the following steps (Fig. 7):

(b) The sample, with the epitaxial side fully processed (step (a) – see also Fig. 6), is bonded onto a sacrificial carrier using a special bonding agent.

(c) The GaAs substrate is removed using a selective wet-etch. The etch-stop layer is then removed using another selective wet-etch, thus exposing the N+ GaAs contact layer. At this stage, the sample is only 10microns thick.

(d) Patterned N-metal pads are evaporated onto the N+ GaAs contact layer. Alloying temperature is minimized to avoid affecting the bonding agent, while still providing an ohmic contact. These bonding pads are then plated with Gold.

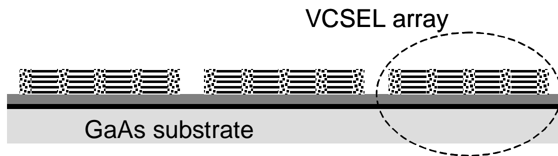
(e) The individual arrays are cleaved. Each array is still attached to its individual sacrificial carrier.

(f) Each array/carrier assembly is then soldered to a high-conductivity submount (such as diamond).

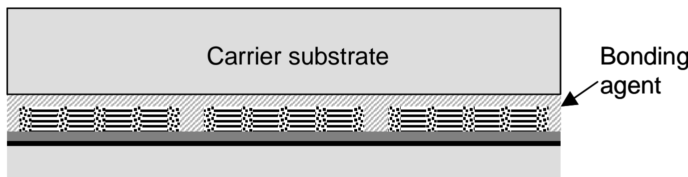
(g) The sacrificial carrier is removed and the array-on-submount assembly is cleaned.

(h) The array is wire-bonded and tested.

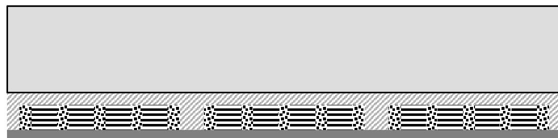
(a) VCSEL sample with processed epitaxial side



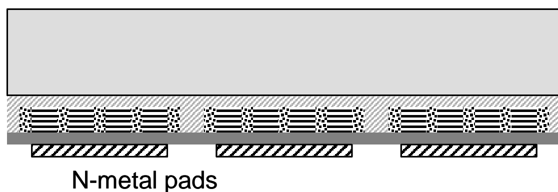
(b) Sample bonded to carrier substrate



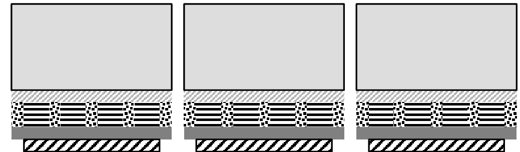
(c) Substrate and etch-stop layer removal



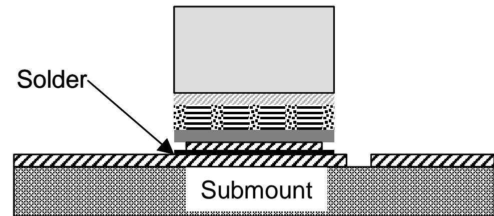
(d) Processing of N-metal bonding pads



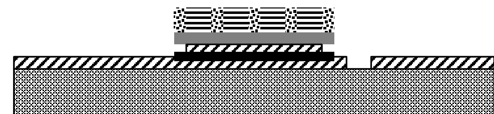
(e) Cleaving of individual VCSEL arrays



(f) Die-attach onto submount



(g) Carrier substrate removal



(h) Wire-bonding and testing

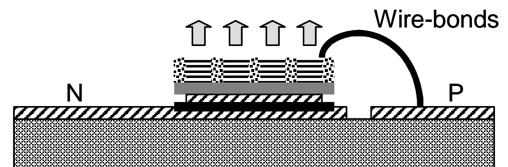


Fig. 7. Processing and packaging steps for 808nm VCSEL arrays. The chip soldered on the submount is only 10microns thick.

Even though the chips are very thin (10microns), we successfully soldered them on diamond submounts. The chip-on-submount can be further packaged onto a micro-channel cooler to increase the heat removal capacity, especially for CW operation.

4. 808NM VCSEL ARRAY RESULTS

Figure 8(a) shows a fully packaged 3mm x 3mm 808nm VCSEL array on diamond submount. The emission area is 2.8mm x 2.8mm and has approximately 3,000 elements. The LIV results are shown in Fig. 8(b). The array rolls over at 58W output power at 70A. A peak PCE of 42% is achieved at 17W (18A).

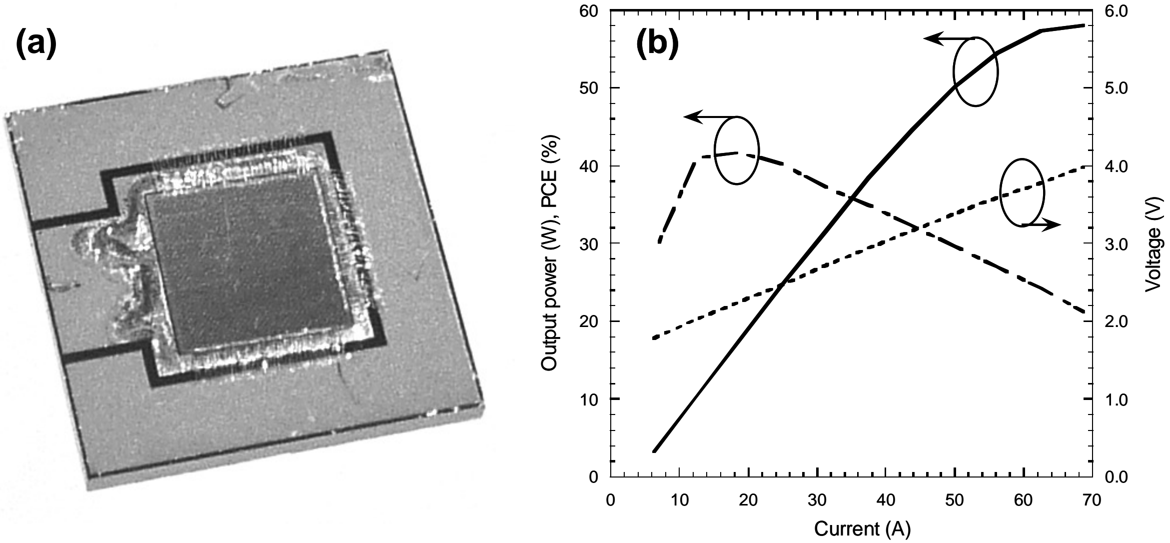


Fig. 8. (a) Photograph of a fully packaged 808nm VCSEL array on diamond submount. The chip is 3mm x 3mm and the emission area is 2.8mm x 2.8mm. (b) LIV characteristics of the chip.

Figure 9 shows the LIV results for a 5mm x 5mm 808nm VCSEL array. The emission area is 4.8mm x 4.8mm and has approximately 10,000 elements. Output power exceeds 120W (125A). A peak PCE of 42% is achieved at 27W (31A).

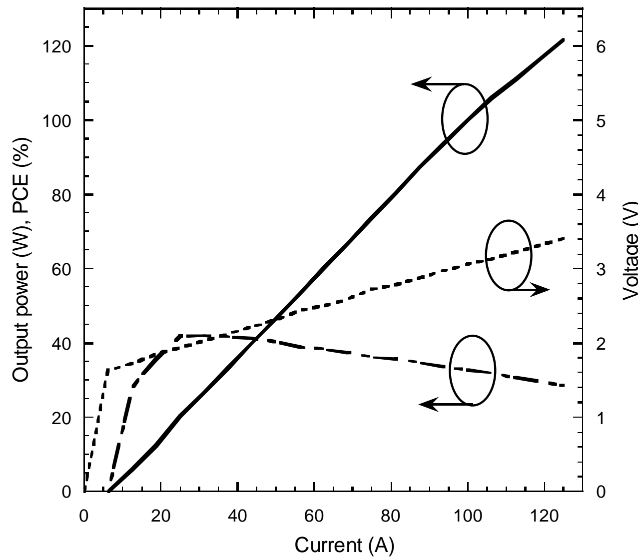


Fig. 9. LIV characteristics of a 5mm x 5mm 808nm VCSEL array.

5. CONCLUSIONS

For high-power, high-efficiecy 808nm VCSEL arrays, multimode devices with a record PCE (49%) were developed. This PCE number is similar to previous results for bottom-emitting 976nm VCSELs and we think VCSELs with such PCE levels can be fabricated across a wide wavelength range (790~1100nm). For higher brightness arrays, single-mode 808nm VCSEL devices were demonstrated with a maximum single-mode power of 4.7mW and a maximum PCE of 42% (at 1.2mW).

For the fabrication of 808nm VCSEL arrays, a process was developed in which the GaAs substrate is completely removed and the chips are soldered onto diamond submounts for efficient heat removal. Two different size arrays were fabricated: 3mm x 3mm and 5mm x 5mm, with output powers in excess of 50W and 120W, respectively, and with peak PCE's of 42%.

These high-power 808nm VCSEL arrays are good candidates for many pumping-based applications.

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